



Update on SEU Detection

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- Finishing up DTC2 layout
- Physics simulations still pending...
- 2nd week of March onwards: focus on SEU detection
- Two questions:
 - 1p6m vs 1p9m?
 - Value of stand-alone bulk CMOS detectors?



- Consequence of charge-redistribution SAR: perturbed charge on the sum node **stays** during the entire conversion cycle.
- Each “detector bit” corresponds to a specific bit of the SAR
 - e.g. for proof of concept, we choose to monitor bits LSB, LSB+1, LSB+2, etc.
- For now: parallel (analog) readout per “detector bit”
- Synchronized to ADC clock (40MSPS)
- At end of each sampling interval:
 - ADC code
 - Analog signal representing perturbed charge from SEU per bit

1p6m vs 1p9m?

- Chen-Kai and I are still hopeful for 1p9m
- Less parasitics, easier routing
- Impossible to stack two MOM-caps in 6 metals
- Use of MOS-caps for SEU detection
 - Ideal to first compare with MOM-caps for SEU detector
 - MOM and MOS based caps will both be implemented in 9 metals
 - MOS cap and 6 metal may be used in future, ideally once effect on MOM caps are known (in 9 metals)

- Research value in investigating capacitor structures for radiation detection, in general?
- Research value in implementing in bulk CMOS over exotic processes?
- If yes: do we have enough resources for an additional chip with just an array of detectors/diodes/dosimeters?

- SAR design (mostly before ~March 15)
 - finish layout
 - Reference buffer? (if there is time at the end)
- Rad-Cal
 - Geant4 physics simulations
 - Design sensors & SAR cap layout